

Lecture 13

Routing Techniques in Network On Chip



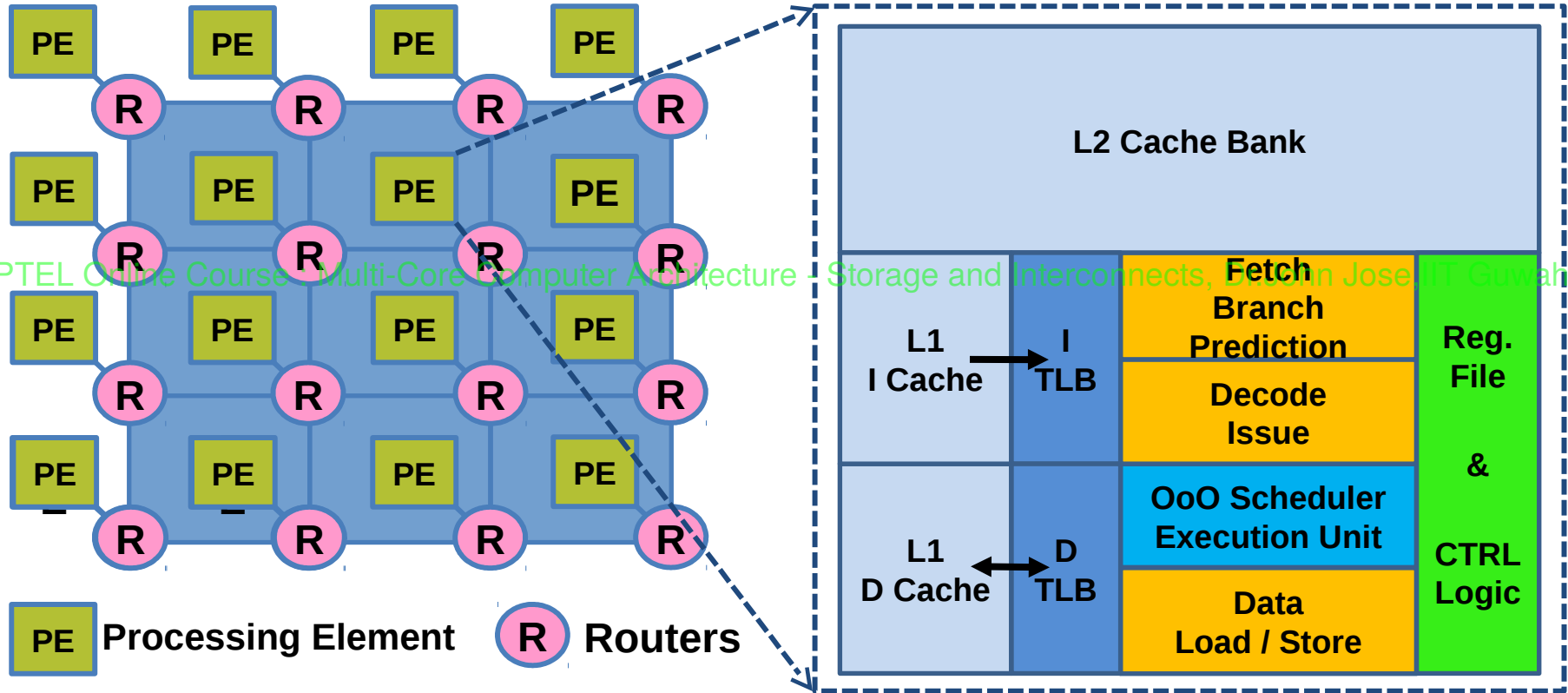
NPTEL Online Course : Multi-Core Computer Architecture - Storage and Interconnects, Dr. John Jose, IIT Guwahati

Dr. John Jose

Assistant Professor

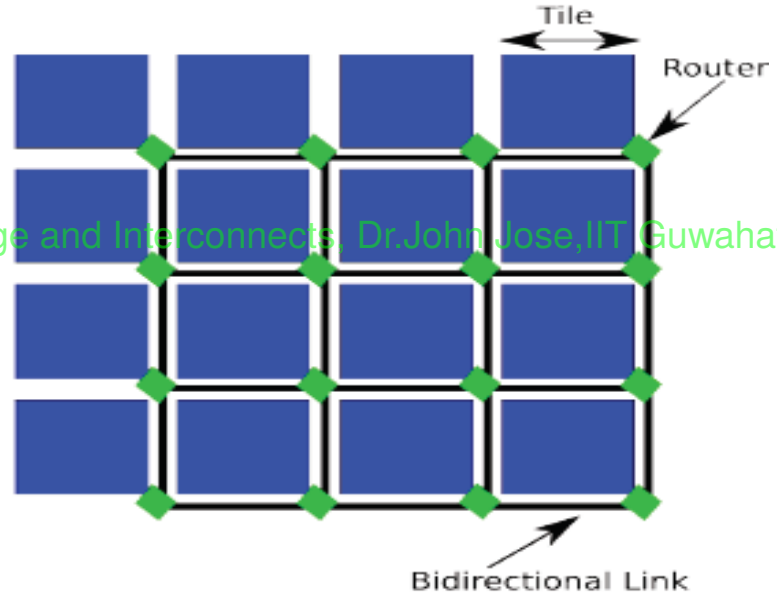
**Department of Computer Science & Engineering
Indian Institute of Technology Guwahati, Assam.**

Tiled Chip Many-Core Processor (TCMP)

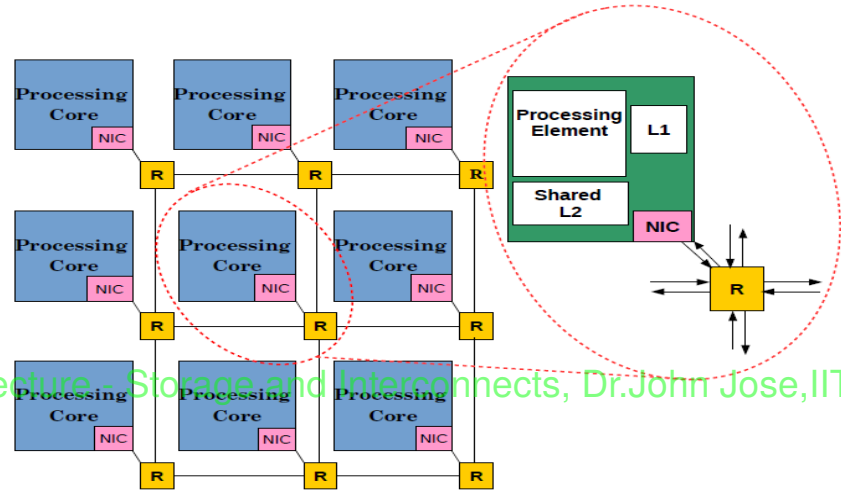
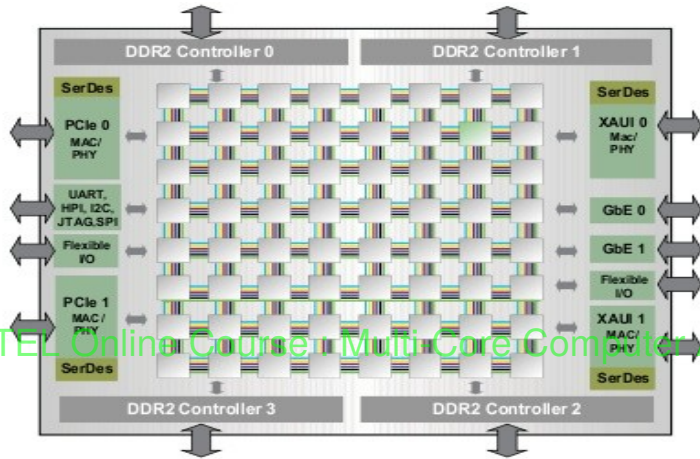


What is NoC ?

- ❖ Processing units interconnected via packet based network
- ❖ Each resource is called as a ***'tile'***
- ❖ All resources organized as rectangular tiles on the chip.
- ❖ Tiles interconnected by network of routers

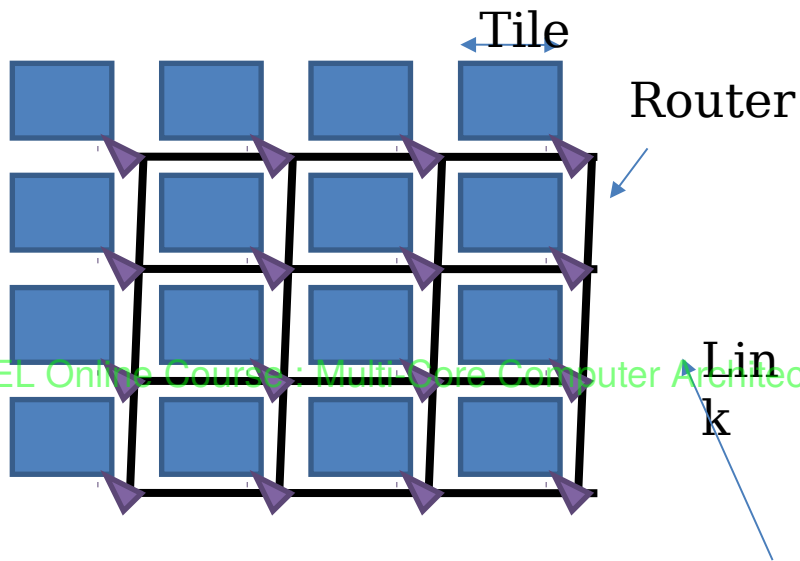


Routers and Tiles



- ❖ East, West, North and South neighbors
- ❖ Packets are divided into flow control units called flits
- ❖ L1 and L2 cache misses create NoC traffic packets

Building Blocks of NoC



❖ **Topology**

❖ **Routing**

❖ **Flow control**

❖ **Router micro-architecture**

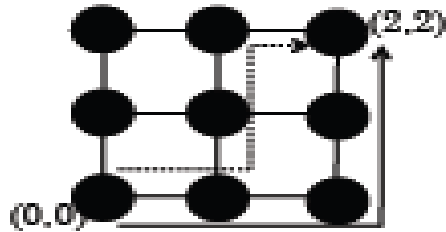
Routing Algorithm

- ❖ Compute the path route for packets to reach destination.
- ❖ **Deterministic:** always chooses the same path for a communicating source-destination pair
- ❖ **Oblivious:** chooses different paths, without considering network state
- ❖ **Adaptive:** can choose different paths, adapting to the state of the network
- ❖ Minimal Routing vs Non-Minimal Routing
- ❖ Source Routing vs Node Routing
- ❖ Deterministic Routing vs Adaptive Routing

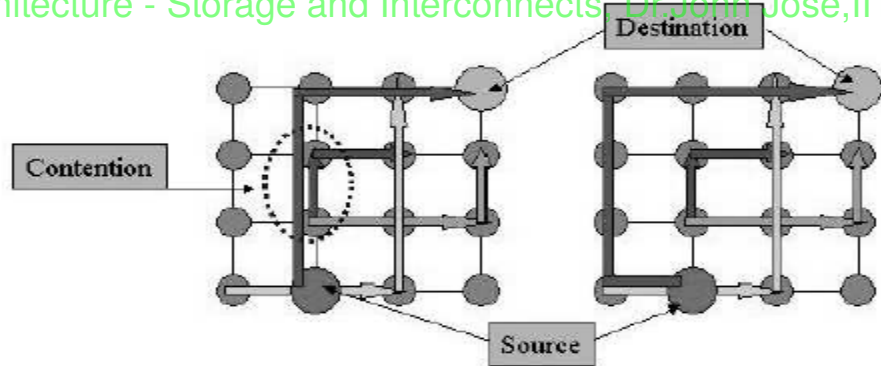
Minimal & Non-Minimal Routing

- ❖ **Profitable route:** The route that always leads the packet closer to the destination.
- ❖ **Misroute:** A route that leads the packet away from the destination.

NPTEL Online Course : Multi-Core Computer Architecture - Storage and Interconnects Dr John Jose, IIT Guwahati

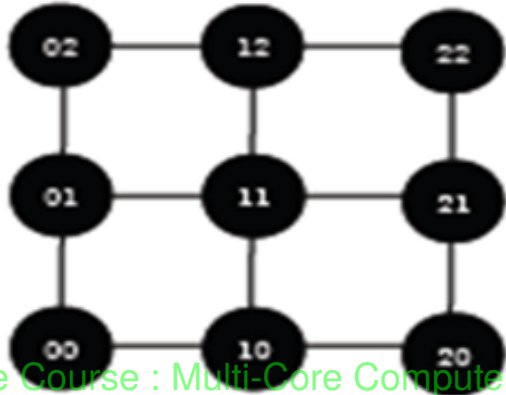


Minimal routing



Non-Minimal routing

Source Routing



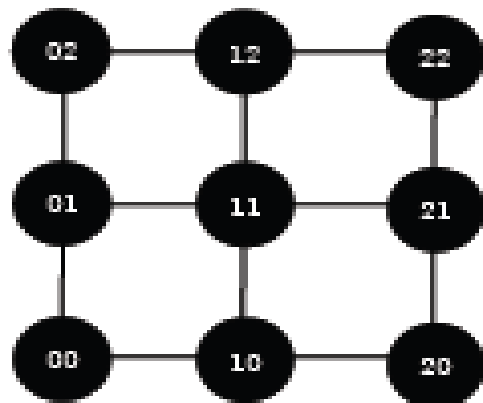
- ❖ Route is embedded in the packet header.
- ❖ Can reduce packet processing delay in nodes.
- ❖ Routing table storage overhead at each node.

Source routing table at Node (0, 0)		
Destination	Route 0	Route 1
00	X	
10	EX	
20	EEX	
01	NX	
11	NEX	ENX
21	NEEX	ENEX
02	NNX	
12	ENNX	NENX
22	EENNX	NNEEX

Node Routing

Node-based routing table for a 3×3 mesh with West-First turn model

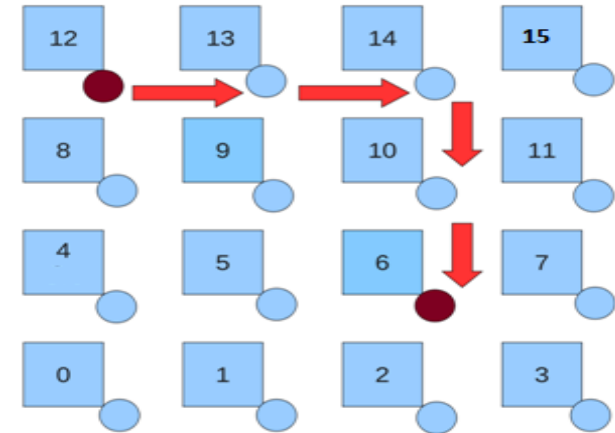
	00	01	02	10	11	12	20	21	22
00	X	N-	N-	E-	EN	EN	E-	EN	EN
01	S-	X	N-	ES	E-	EN	ES	E-	EN
02	S-	S-	X	ES	ES	E-	ES	ES	E-
10	W-	W-	W-	X	N-	N-	E-	EN	EN
11	W-	W-	W-	S-	X	N-	ES	E-	NE
12	W-	W-	W-	S-	S-	X	ES	ES	E-
20	W-	W-	W-	W-	W-	W-	X	N-	N-
21	W-	W-	W-	W-	W-	W-	S-	X	N-
22	W-	W-	W-	W-	W-	W-	S-	S-	X



- ❖ Compute next outgoing port at each hop
- ❖ Small routing table / logic at each node
- ❖ Can incorporate dynamic network conditions
- ❖ Delay in identifying next link due to table lookup

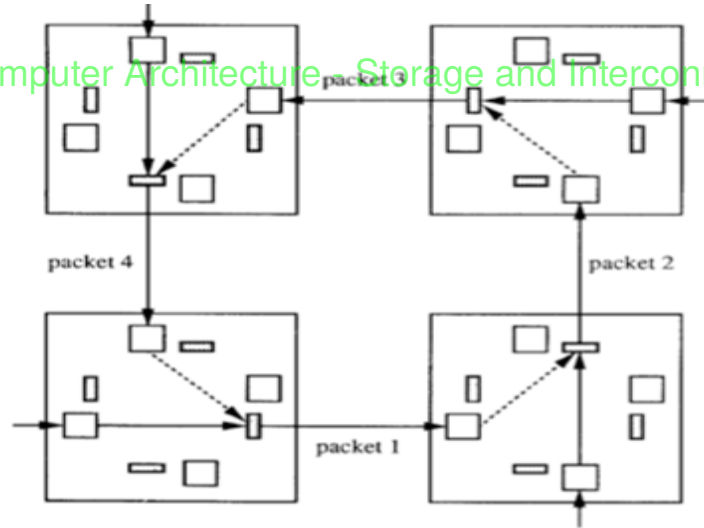
Deterministic Routing

- ❖ All packets between the same (source, dest) pair take the same path
- ❖ Dimension-order routing – Eg. XY routing
 - ❖ First traverse dimension X, then traverse dimension Y
 - ❖ Simple
 - ❖ Deadlock freedom
 - ❖ Could lead to high contention
 - ❖ Does not exploit path diversity



Deadlock

- ❖ No forward progress
- ❖ Caused by circular dependencies on resources
- ❖ Each packet waits for a buffer occupied by another packet downstream

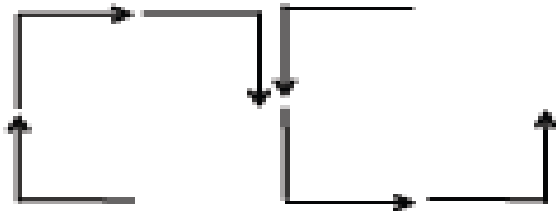
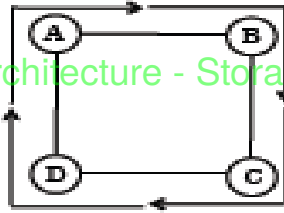


Handling Deadlock

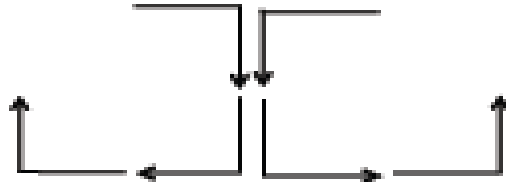
- ❖ Avoid cycles in routing - Dimension order routing cannot build a circular dependency
- ❖ Restrict the turns each packet can take
- ❖ Avoid deadlock by adding more buffering (escape paths)
- ❖ Detect and break deadlock by preemption of buffers

Turn Model to Avoid Deadlock

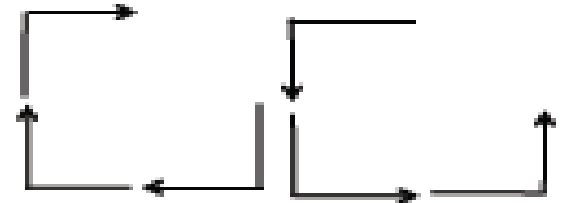
- ❖ Analyze directions in which packets can turn in the network
- ❖ Determine turns they can form cycles
- ❖ Prohibit just enough turns to break possible cycles



West First Turns

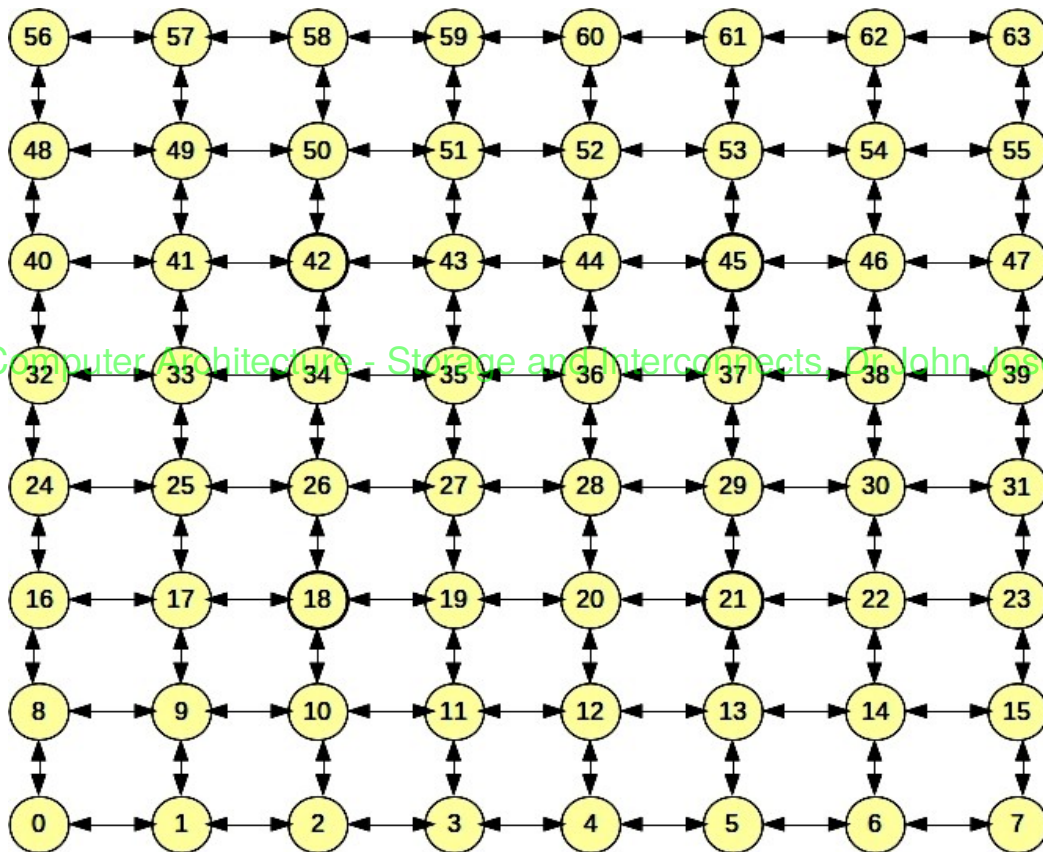
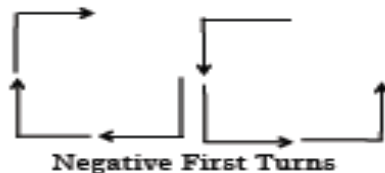
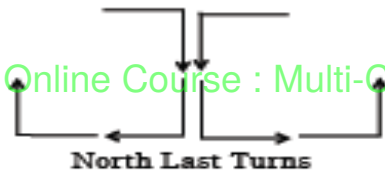
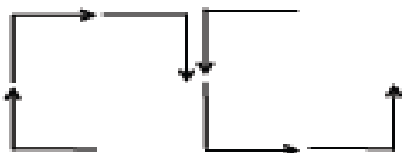


North Last Turns

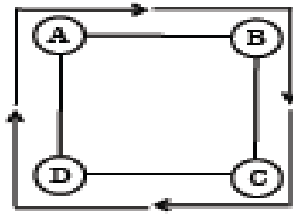


Negative First Turns

Turn Model to Avoid Deadlock

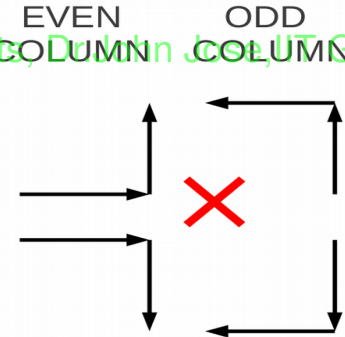
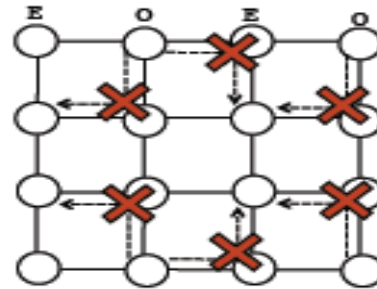
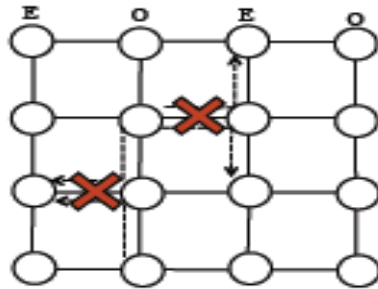


Adaptive Odd-Even Turn Routing

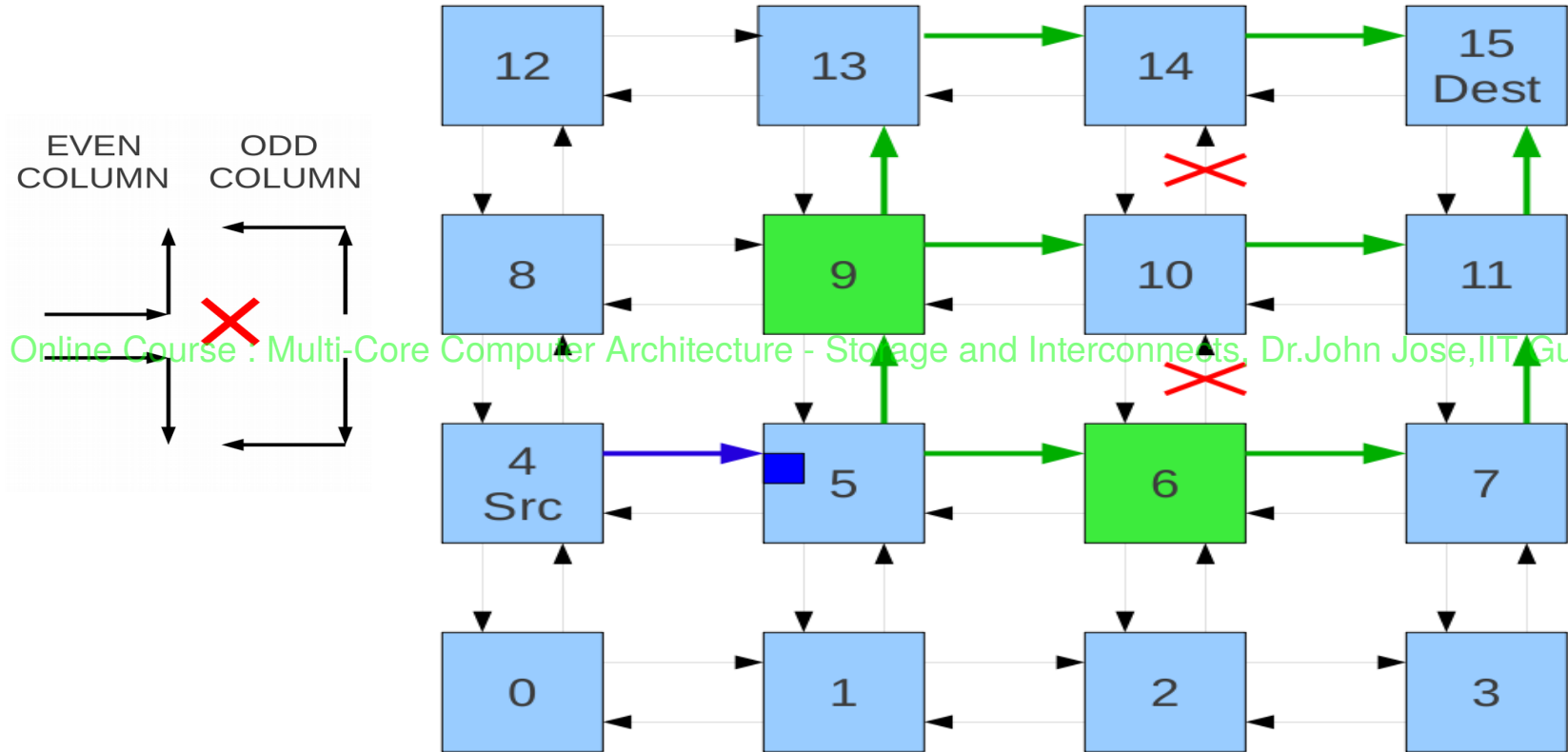


**Non restrictive turns
leads to deadlocks**

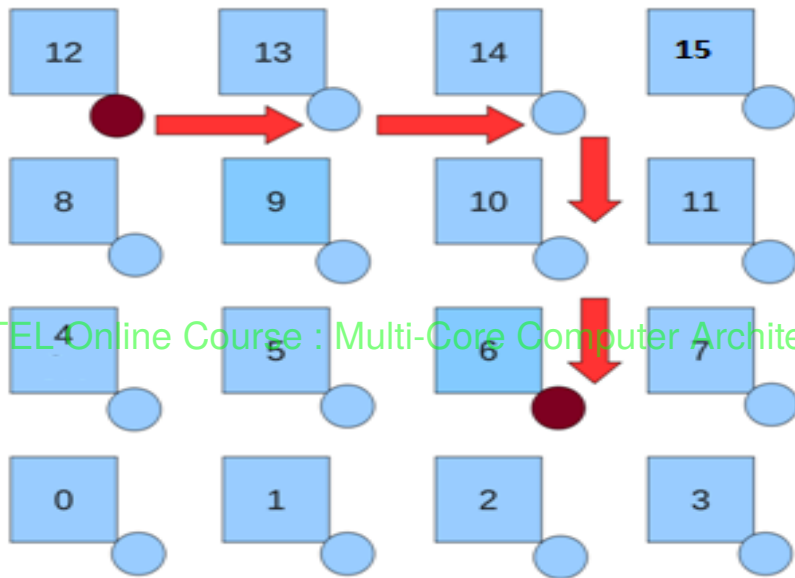
- ❖ Prohibited Turns at certain junctions
- ❖ For nodes in even column EN and ES.
- ❖ For nodes in odd column NW and SW.



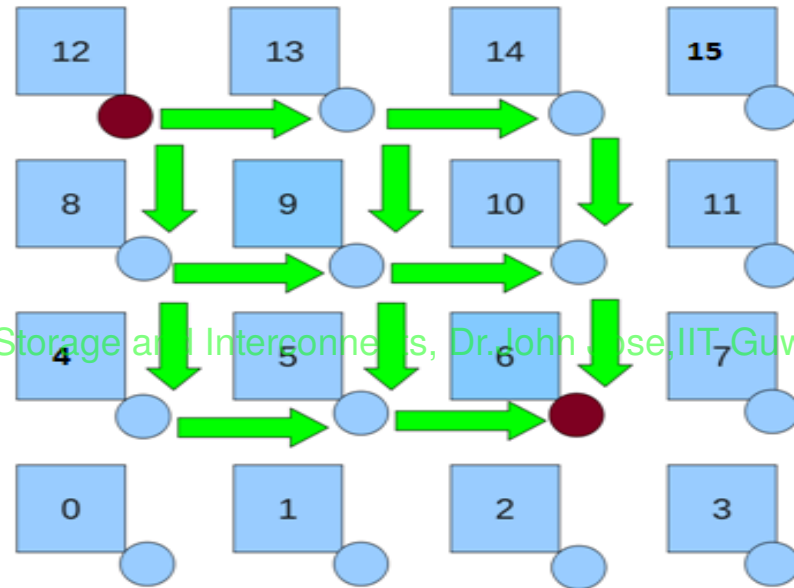
The Minimal Odd-Even Routing



Static vs Adaptive Routing



Static routing - XY routing



Adaptive Routing

Adaptive Routing

❖ Minimal adaptive

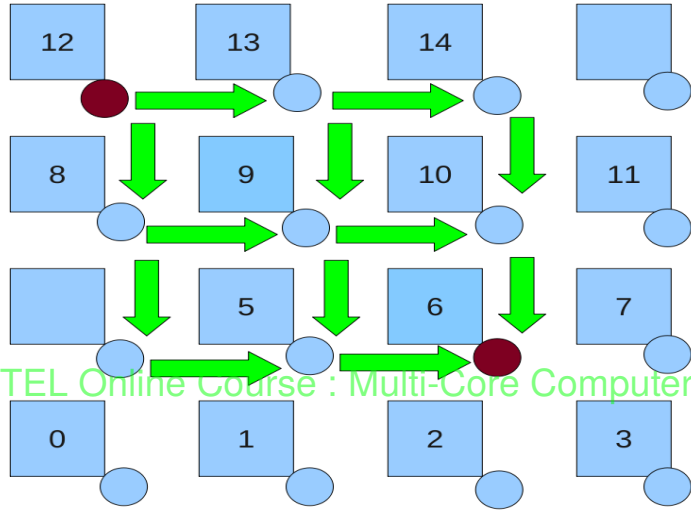
- ❖ Router uses network state (e.g., downstream buffer occupancy) to pick which productive output port to send
- ❖ Productive output port - port that gets the packet closer to its destination
- ❖ Aware of local congestion
- ❖ Restricts achievable link utilization & load balance

Adaptive Routing

- ❖ Non-minimal (fully) adaptive

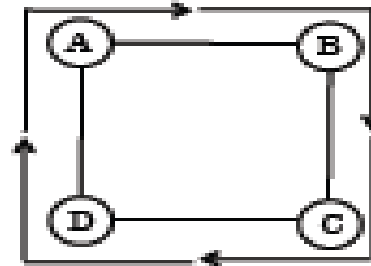
- ❖ Misroute packets to non-productive output ports also based on network state
- ❖ Can achieve better network utilization and load balance
- ❖ Need to guarantee livelock freedom

Adaptive Routing



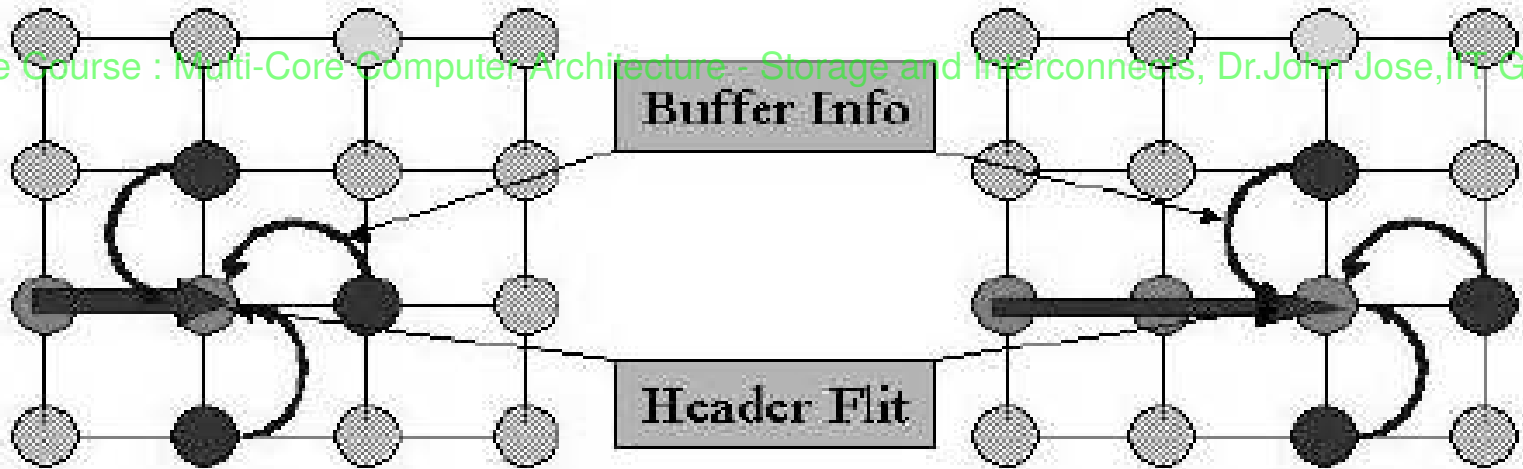
Minimal- Adaptive Routing

- ❖ Local and global information can be exploited for route selection.
- ❖ Preserving inter message order and out of order delivery.
- ❖ Should be deadlock and livelock free.



Contention-look-ahead Routing

- ❖ Can foresee the contention of neighbors using control wires.
- ❖ The traffic condition of the neighboring nodes are obtained through the control signal wires.



**THANK
YOU!**

FOR

YOUR

PRESENCE

NPTEL Online Course : Multi-Core Computer Architecture - Storage and Interconnects, Dr. John Jose, IIT Guwahati

johnjose@iitg.ac.in

<http://www.iitg.ac.in/johnjose/>